

FROM A CIRCUIT
OF THE PRECEDING
STEP

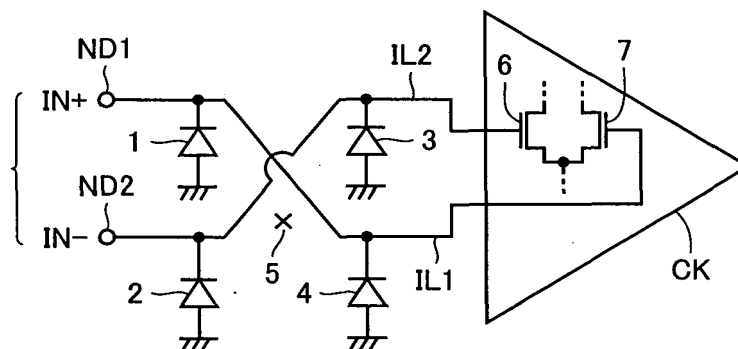


FIG.2

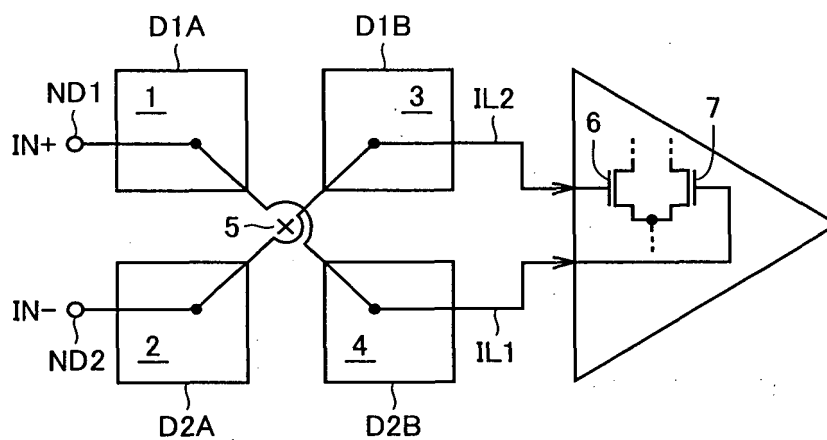


FIG.3

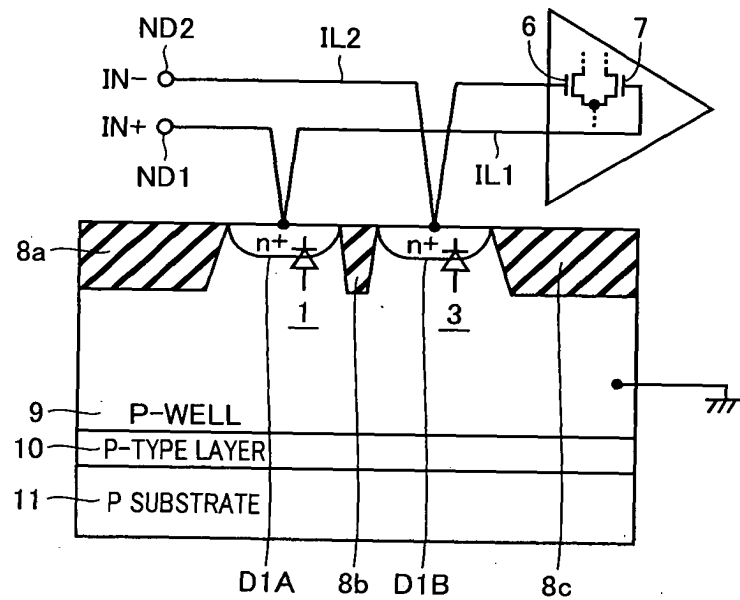


FIG.4

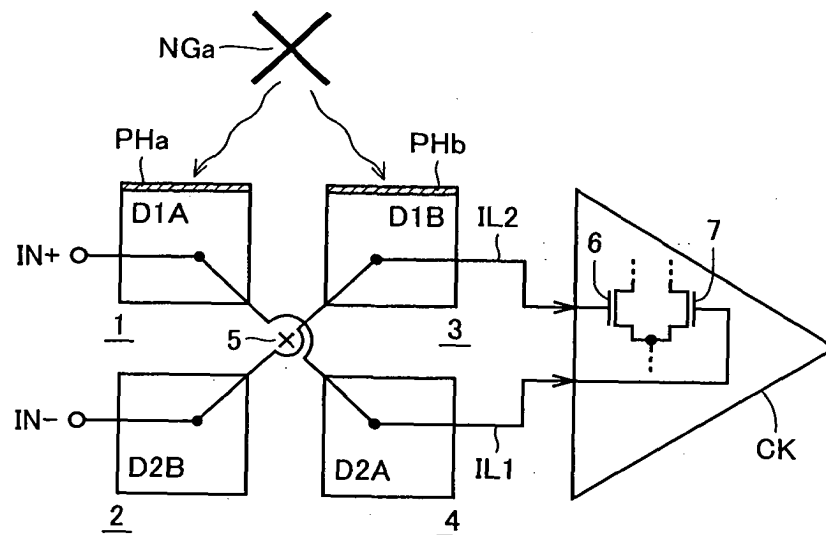


FIG.5

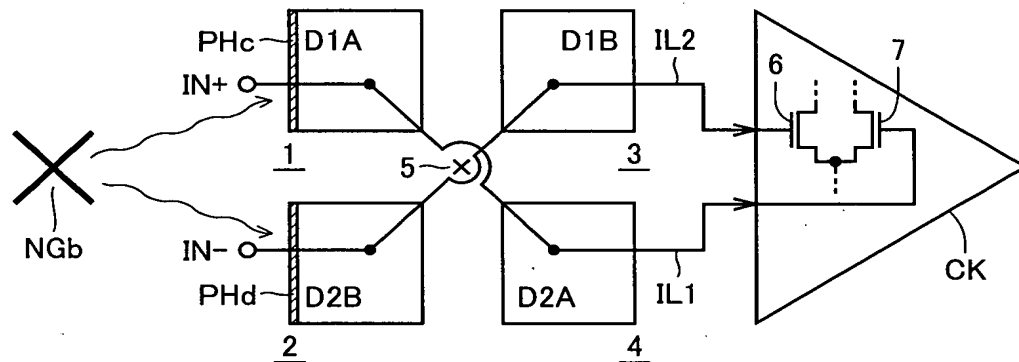


FIG.6

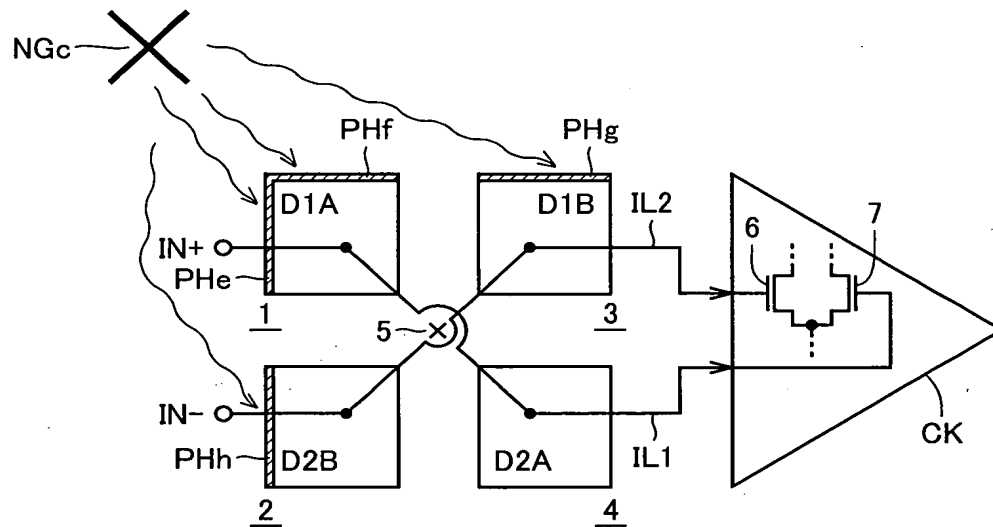


FIG.7

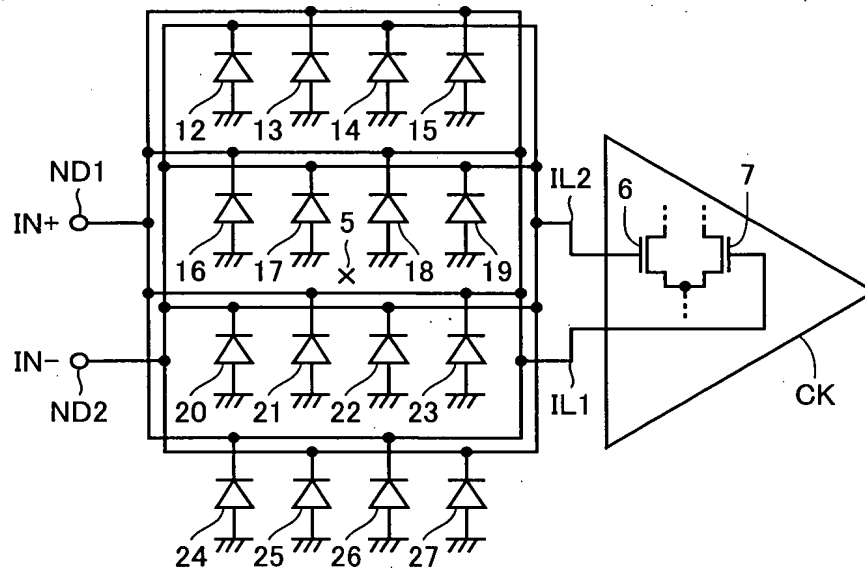


FIG.8

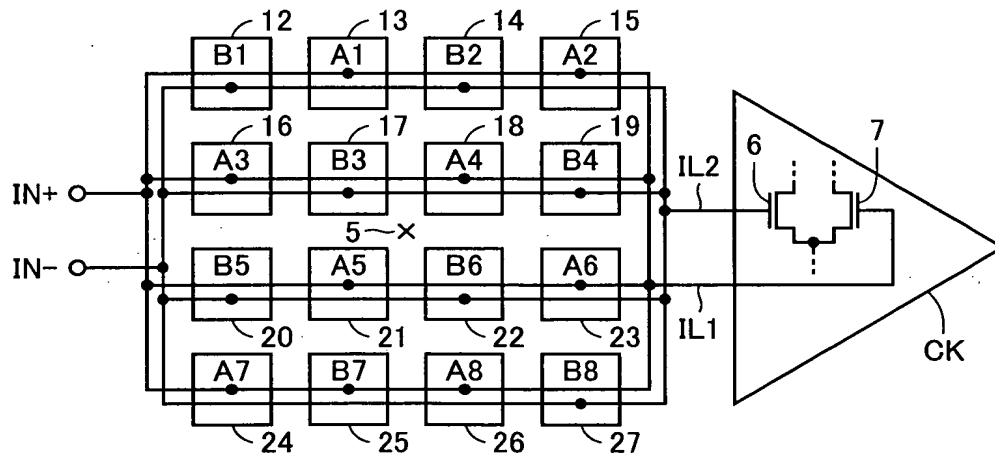


FIG.9

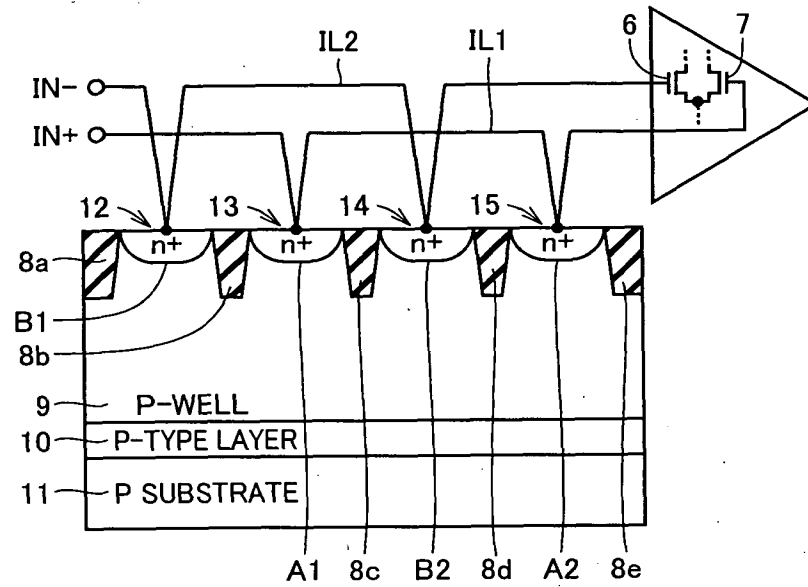


FIG.10

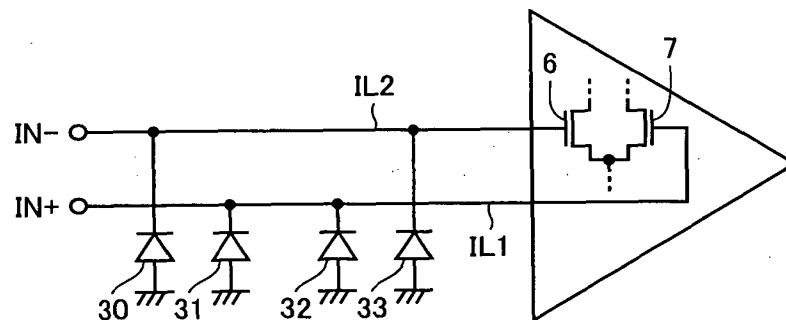


FIG.11

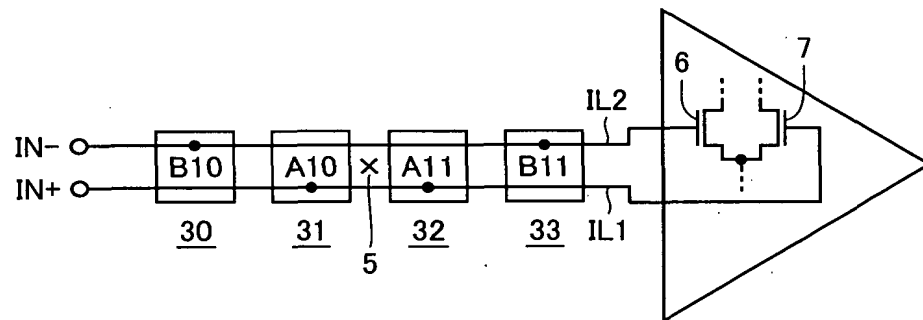


FIG.12

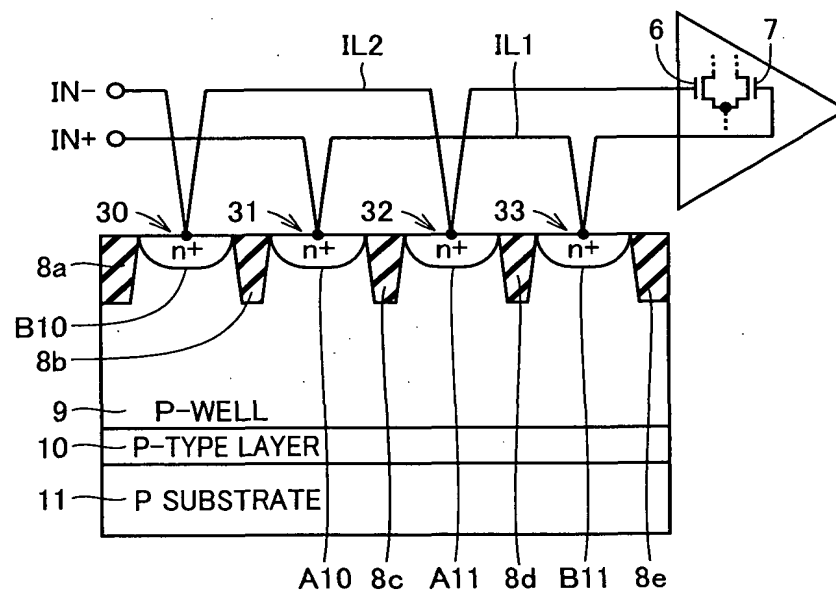


FIG.13

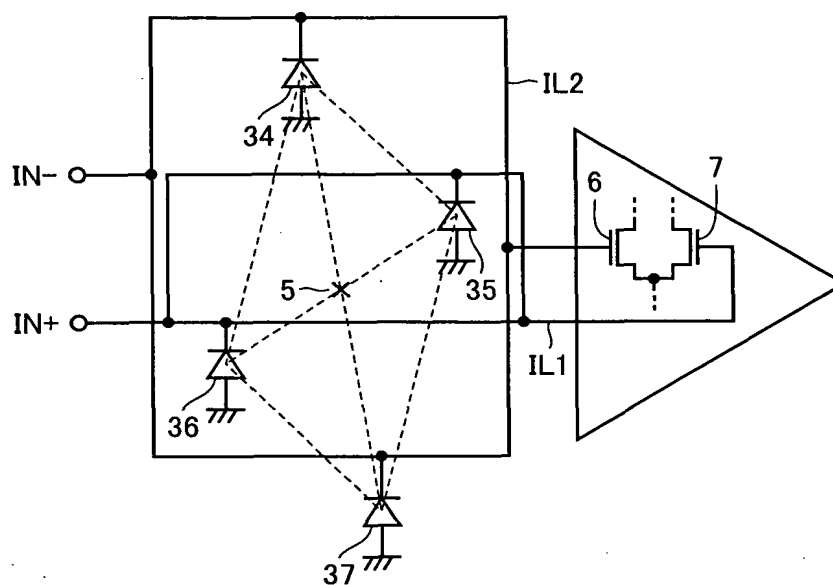


FIG.14

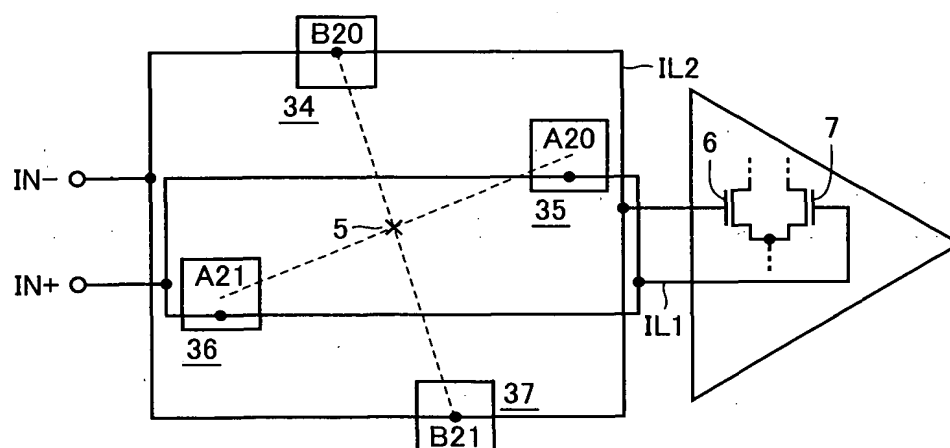


FIG.15

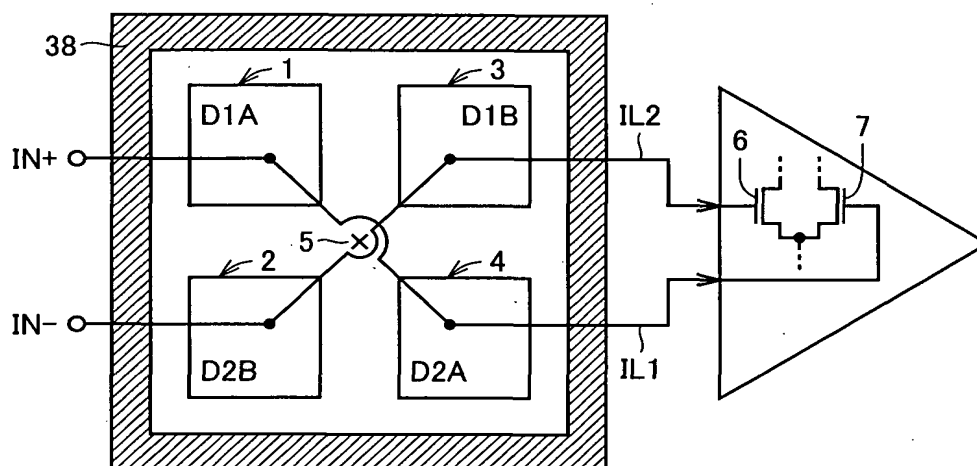


FIG.16

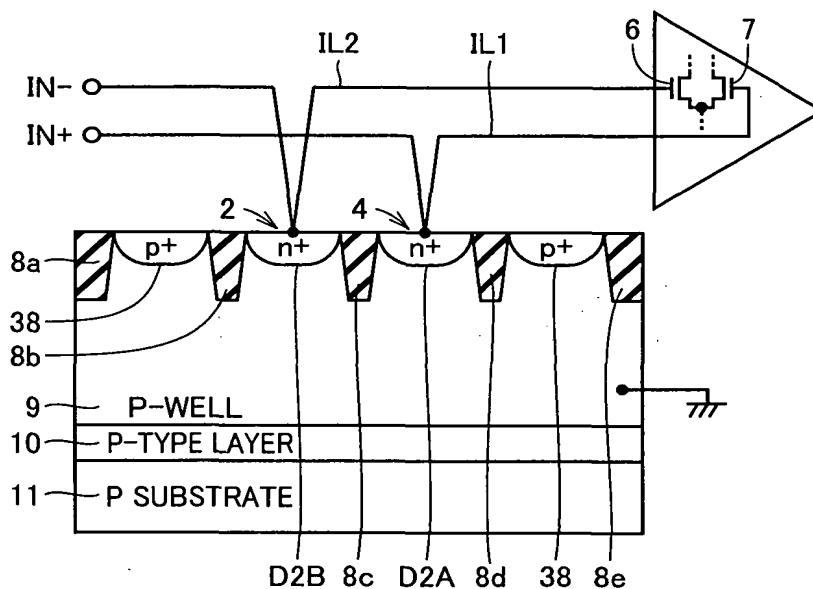


FIG.17

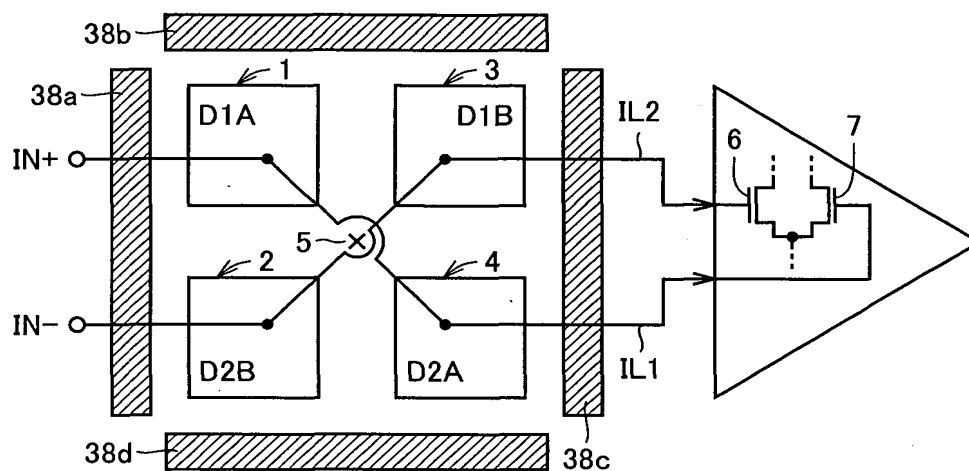


FIG.18

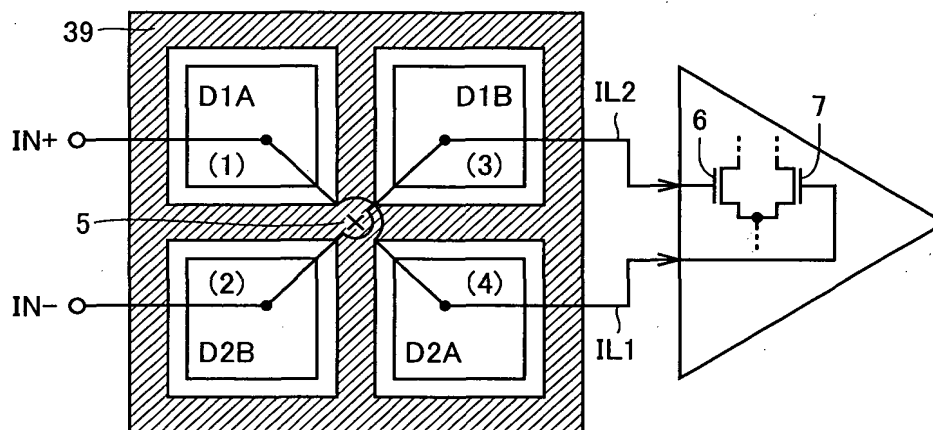


Figure 1 is a schematic diagram of a differential signal processing circuit. The circuit includes two input terminals, IN+ and IN-, each connected to a pair of differential input transistors (D1A, D1B and D2A, D2B). These transistors are connected to a central node (5) which is connected to a differential output stage (6, 7). The output stage is connected to a load resistor (39a) and a feedback resistor (39b). The circuit is biased by a current source (39c) and a differential pair of transistors (39d, 39e).

FIG.21

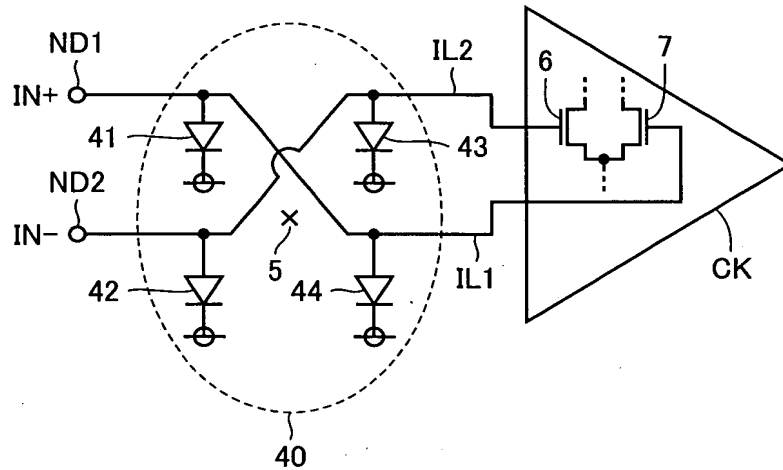


FIG.22

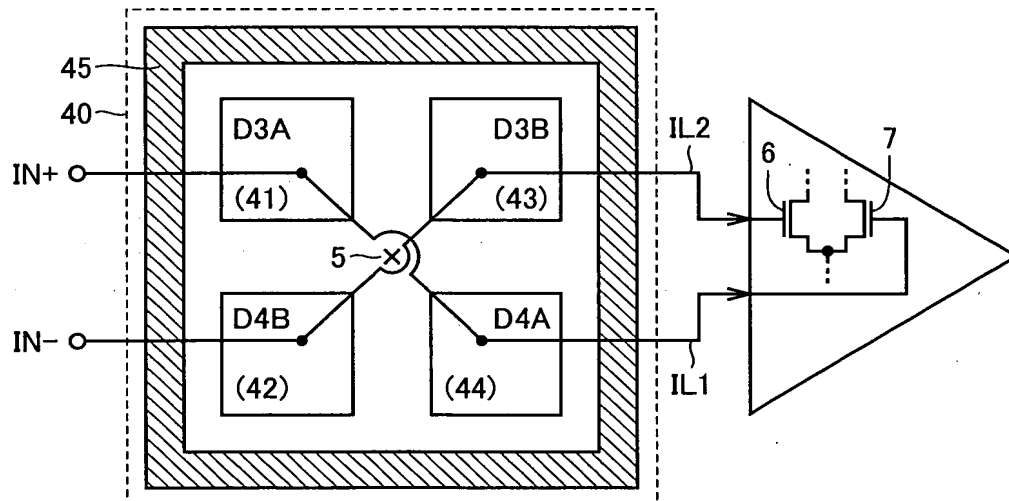


FIG.23

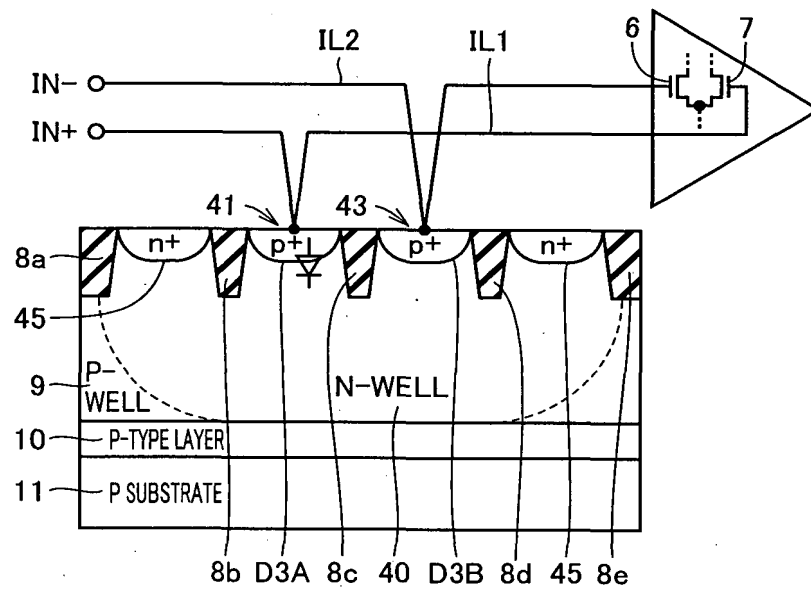


FIG.24

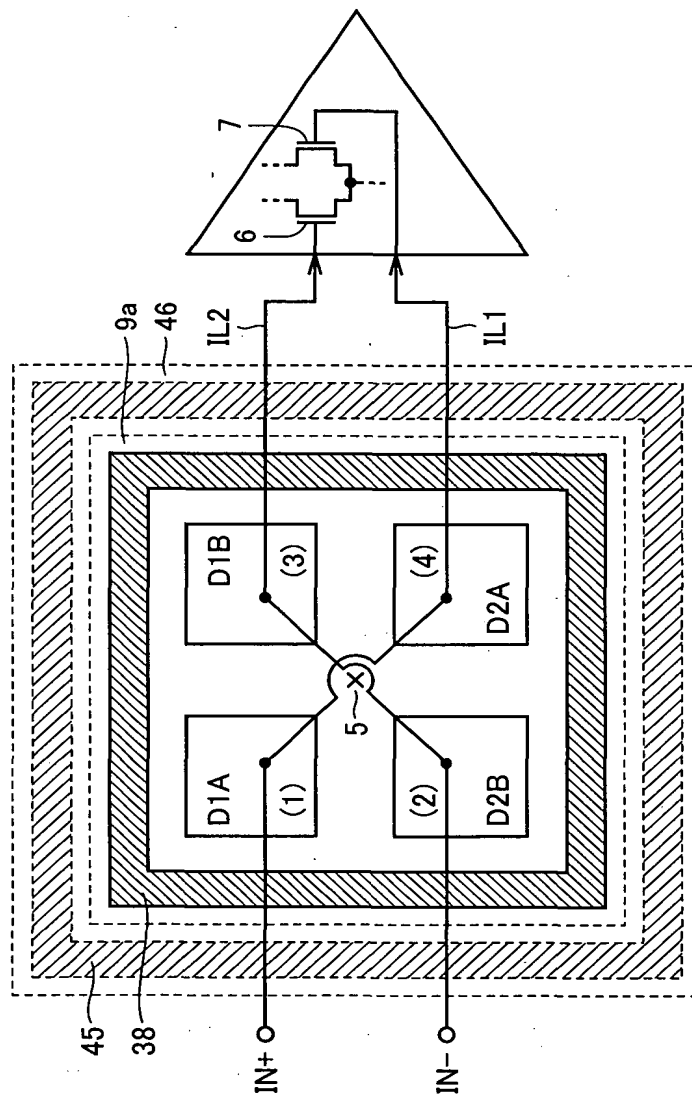


FIG.25

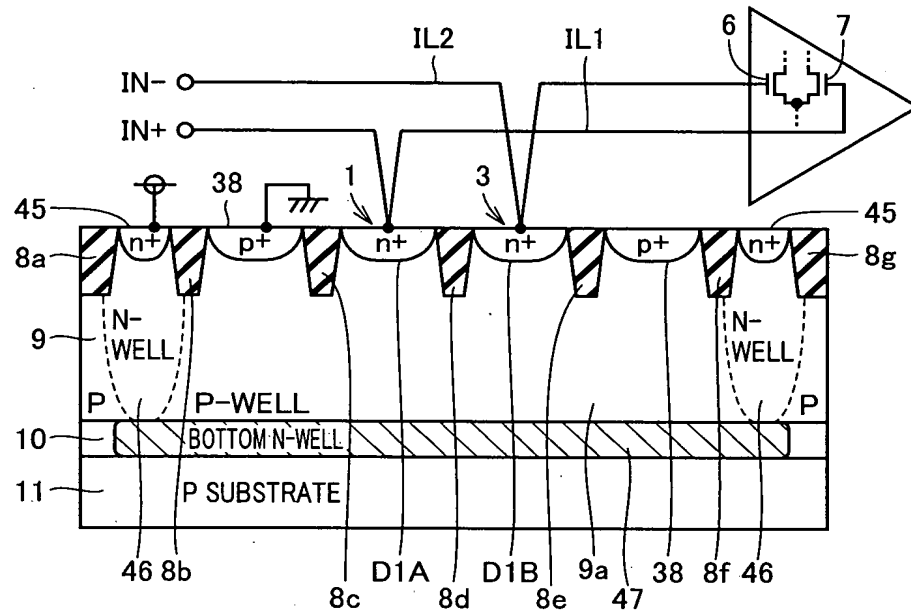


FIG.26

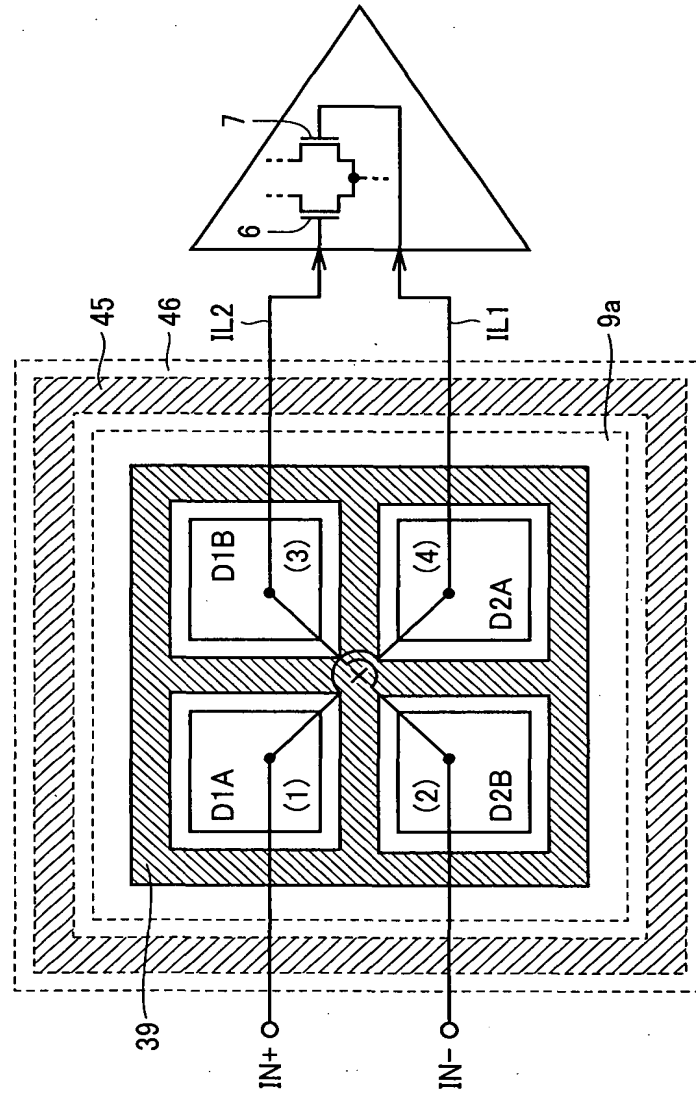


FIG.27

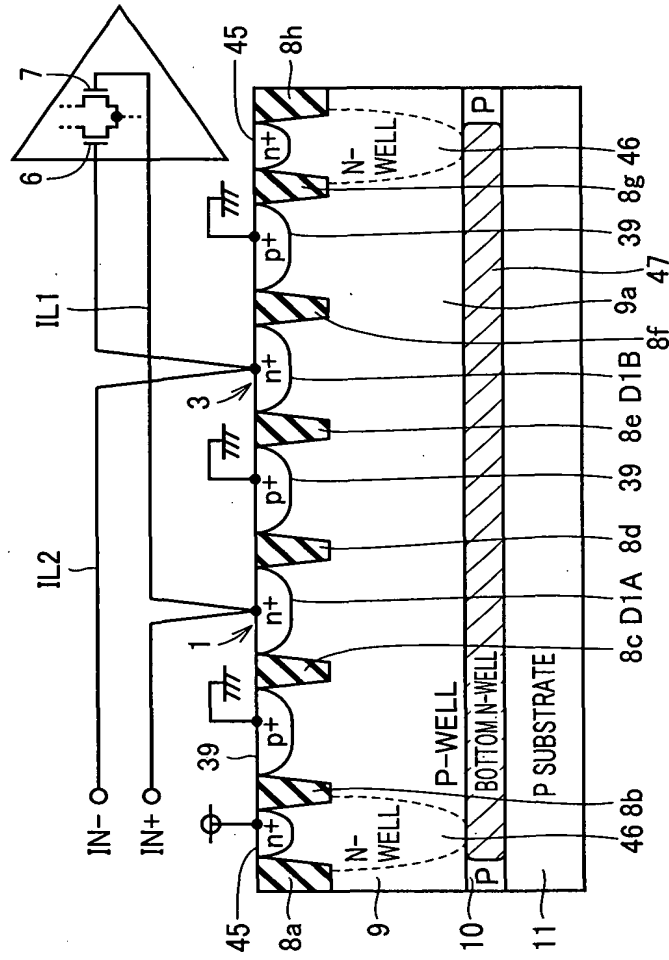


FIG.28

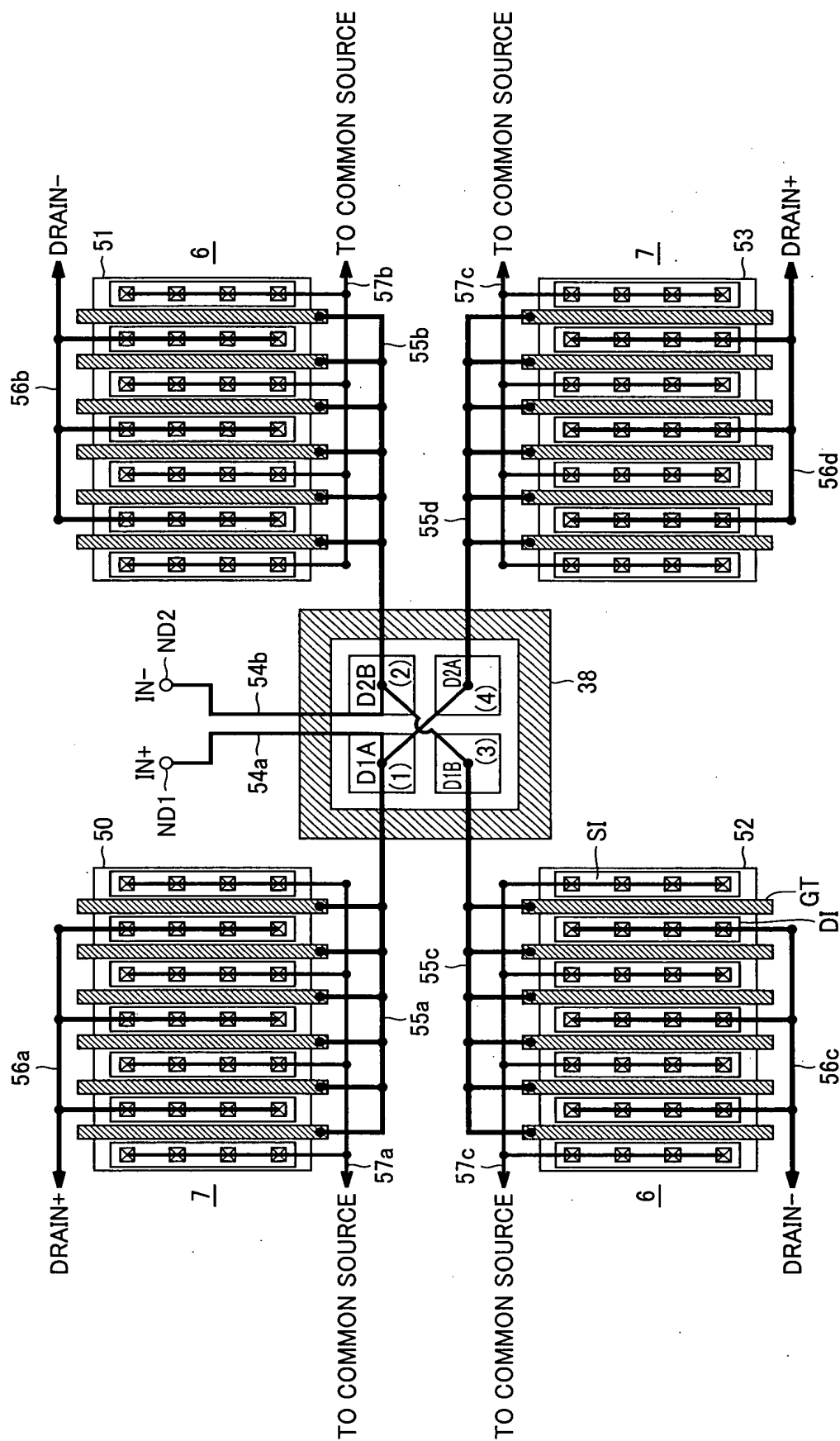


FIG.29

